UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/922,742	08/07/2001	Toshikazu Nakamura	108066-00038	9593

7590 09/09/2004

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
Suite 600
1050 Connecticut Avenue, N.W.
Washington, DC 20036-5339

EXAMINER	
VITAL, PIERRE M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	09/922,742	NAKAMURA, TOSHIKAZU	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 13-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-11* is/are allowed.

6)☒ Claim(s) *13-16 and 19-26* is/are rejected.

7)☒ Claim(s) *17 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 10, 2004 has been entered.

Response to Amendment

2. This Office Action is in response to applicant's communication filed August 10, 2004 in response to PTO Office Action mailed May 18, 2004. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

3. Claims 1-11 and 13-26 have been presented for examination in this application. In response to the last Office Action, claims 13-17 and 19-20 have been amended. Claim 12 has been canceled. Claims 21-26 have been added. As a result, claims 1-11 and 13-26 are now pending in this application.

4. The objection to claim 13 has been withdrawn due to the amendment filed August 10, 2004.

Response to Arguments

5. Applicant's arguments with respect to claims 13-26 have been considered but are moot in view of the new ground(s) of rejection.

6. Applicant's arguments, see pages 14-16, filed August 10, 2004, with respect to the rejection(s)of claim(s) 13-16 and 19-20 under 35USC 102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Ohtake et al (US6,088,290) and Douchi et al (US6,466,075).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 13-16, 19-20 and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtake et al (US6,088,290) and Douchi et al (US6,466,075).

As per claims 13, 19-20, Ohtake discloses a semiconductor integrated circuit comprising a clock buffer for generating an internal clock signal [*clock input buffer circuits 8 and 82 generate internal clock signals CLKIN1, CLKIN2*; col. 1, lines 35-37; Fig. 9]; an input buffer that fetches an input signal in synchronization with said internal clock signal provided from said clock buffer [*all operations of the DRAM are in synchronism with the rising of clock signals supplied to clock signal input pins*; col. 1, lines 22-24].

However, Ohtake does not specifically teach a clock buffer controller that, upon detecting a change in said input signal, activates said clock buffer to generate said internal clock signal and to provide said internal clock signal to said input buffer as recited in the claim.

Douchi discloses a power-down signal input buffer functioning as an external control signal input circuit that activates a clock signal input buffer when a main-power down signal is high so that the validation and invalidation timings of the internal clock changes in accordance with the power-down signal (col. 6, lines 29-58, col. 3, lines 12-14). Since the technology for implementing a clock buffer controller that activates a clock signal input buffer upon detecting a change in an input signal was well known as evidenced by the Douchi reference, and since a clock buffer controller that activates a clock signal input buffer upon detecting a change in an input signal provides for validation and invalidation timings of the internal clock that changes in accordance with the power-down signal, an artisan would have been motivated to implement the above feature in the system of Ohtake. Thus, It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the system of Ohtake to include a clock buffer controller that activates a clock signal input buffer upon detecting a change in an input signal because it was well known to provide for validation and invalidation timings of the internal clock that changes in accordance with the power-down signal as taught by Douchi.

As per claim 14, Ohtake discloses the claimed invention as detailed above in the previous paragraphs. However, Ohtake does not specifically teach a clock buffer controller that compares an input signal with an internal signal output from an input buffer to detect the change in said input signal as recited in the claim.

Douchi discloses a clock buffer controller that compares an input signal with an internal signal output from an input buffer to detect the change in said input signal so that the validation and invalidation timings of the internal clock changes in accordance with the power-down signal (col. 8, lines 29-59, col. 3, lines 12-14). Since the technology for implementing a clock buffer controller that compares an input signal with an internal signal output from an input buffer to detect the change in said input signal was well known as evidenced by the Douchi reference, and since a clock buffer controller that compares an input signal with an internal signal output from an input buffer to detect the change in said input signal provides for validation and invalidation timings of the internal clock that changes in accordance with the power-down signal, an artisan would have been motivated to implement the above feature in the system of Ohtake. Thus, It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the system of Ohtake to include a clock buffer controller that compares an input signal with an internal signal output from an input buffer to detect the change in said input signal because it was well known to provide for validation and invalidation timings of the internal clock that changes in accordance with the power-down signal as taught by Douchi.

As per claim 15, the combination of Ohtake and Douchi discloses the claimed invention as detailed per claim 13 above in the previous paragraphs. Ohtake further discloses a plurality of input buffers [*input buffers 41i*; Fig.2; col. 7, lines 24-29].

As per claim 16, the combination of Ohtake and Douchi discloses the claimed invention as detailed per claim 13 above in the previous paragraphs. The combination of Ohtake and Douchi also provides for a plurality of clock buffer controllers since the signal input buffer which functions as an external control input circuit is included in each of the internal clock signal generating circuits 10a, 10b (see Figs. 4 and 12).

As per claims 24-26, the combination of Ohtake and Douchi discloses the claimed invention as detailed per claim 13 and 15 above in the previous paragraphs. The combination of Ohtake and Douchi also provides for a first and second clock buffers (*buffers 11 and 12*; see Figs 4 and 12 of Douchi).

9. Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtake et al (US6,088,290) and Douchi et al (US6,466,075) and Tomita et al (US6,339,353).

As per claims 21-23, the combination of Ohtake and Douchi discloses the claimed invention as detailed per claim 13 and 15 above in the previous paragraphs. However, the combination of Ohtake and Douchi does not specifically teach an input

signal selected from the group consisting of a command signal and an address signal as recited in the claims.

Tomita discloses an input signal selected from the group consisting of a command signal and an address signal to assure low current consumption and reduce current consumption (col. 1, lines 59-67). Since the technology for implementing an input signal selected from the group consisting of a command signal and an address signal was well known as evidenced by Tomita, and since an input signal selected from the group consisting of a command signal and an address signal assures low current consumption and reduces current consumption, an artisan would have been motivated to implement the above feature in the system of Ohtake and Douchi. Thus, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the system of Ohtake and Douchi to include an input signal selected from the group consisting of a command signal and an address signal because it was well known to assure low current consumption and reduce current consumption as taught by Tomita.

Allowable Subject Matter

10. Claims 1-11 are allowed over the prior art of record.

11. Claims 17-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

As per claims 1, 5 and 11, the prior art of record does not teach or suggest "a clock input buffer supplying an internal clock to a command, address, and data input buffers in normal operation mode, and wherein said clock input buffer supplies said internal clock to said command input buffer and stops supply of said internal clock to said address input buffer or data input buffer in data hold mode" in combination with the other elements set forth in the claimed invention.

Therefore, dependent claims 2-4 and 6-10 are allowable as being dependent upon independent claims 1, 5 and 11 and having additional allowable features therein.

As per claim 17, the prior art of record does not teach or suggest "a signal change monitoring circuit including a comparative circuit that compares an input signal with signal output from an input buffer, and wherein a clock buffer controller further includes a logic circuit that logically synthesizes signals output from a plurality of said comparative circuits, generates an activation signal that activates said clock buffer, and supplies the activation to said clock buffer" in combination with the other elements set forth in the claimed invention.

Therefore, dependent claim 18 is allowable as being dependent upon independent claim 17 and having additional allowable features therein.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach SDRAM operating in synchronism with external clock, clock input buffer operating in normal operation mode or data hold mode and activating clock buffer when there is change in input signal supplied to input buffer.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

September 5, 2004

Pierre M. Vital
Examiner
Art Unit 2188